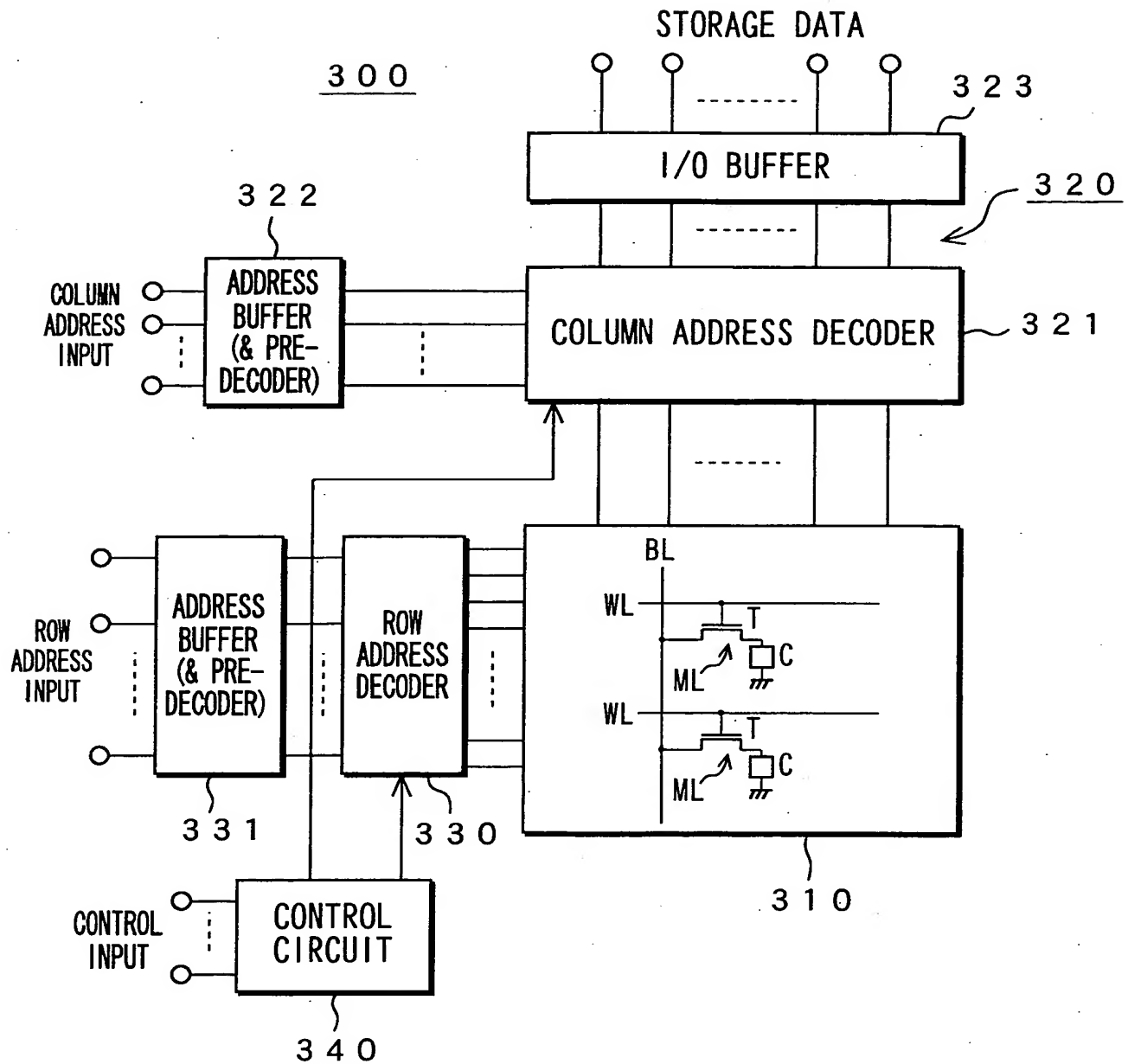


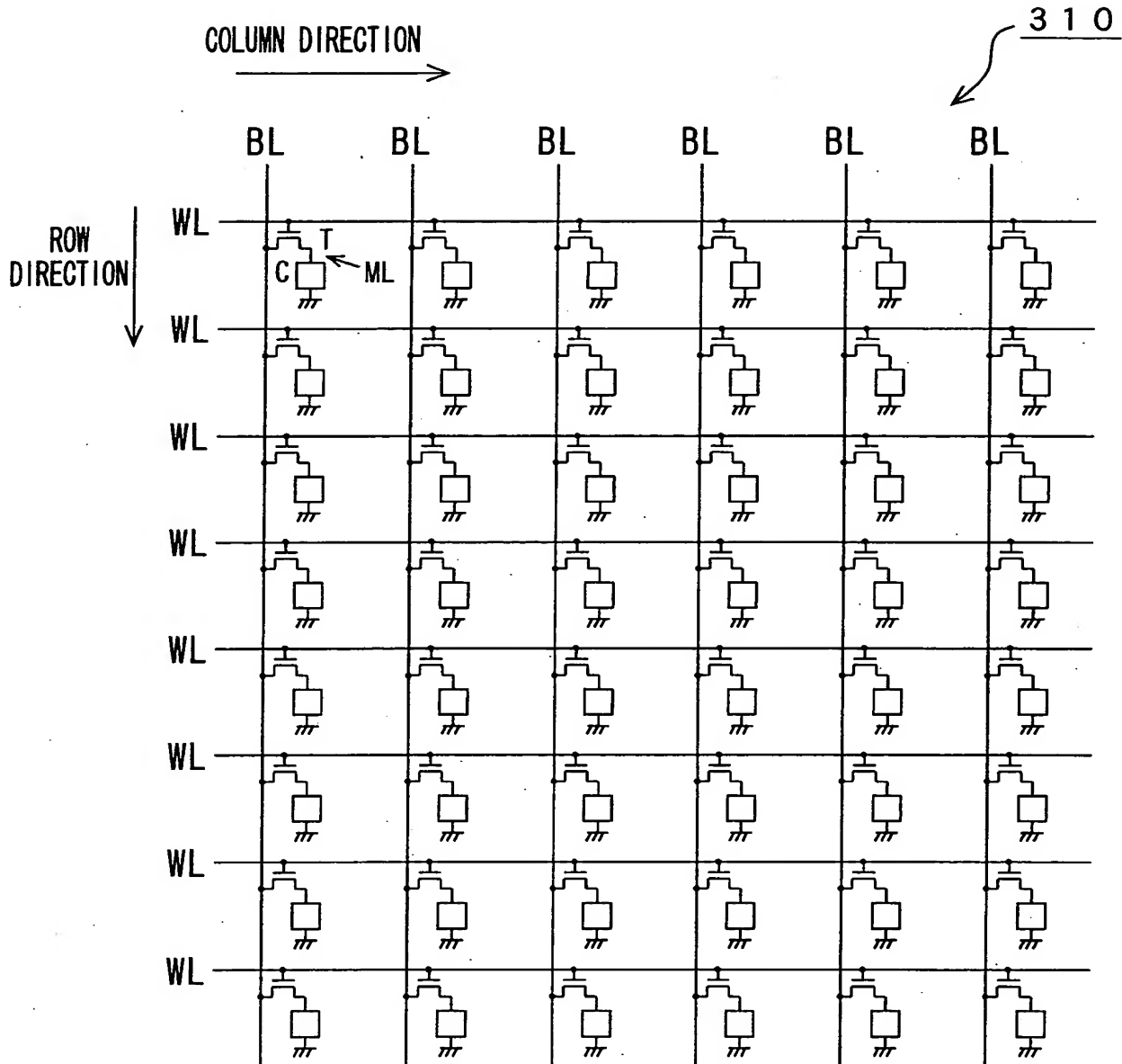
1 / 2 3

F I G . 1



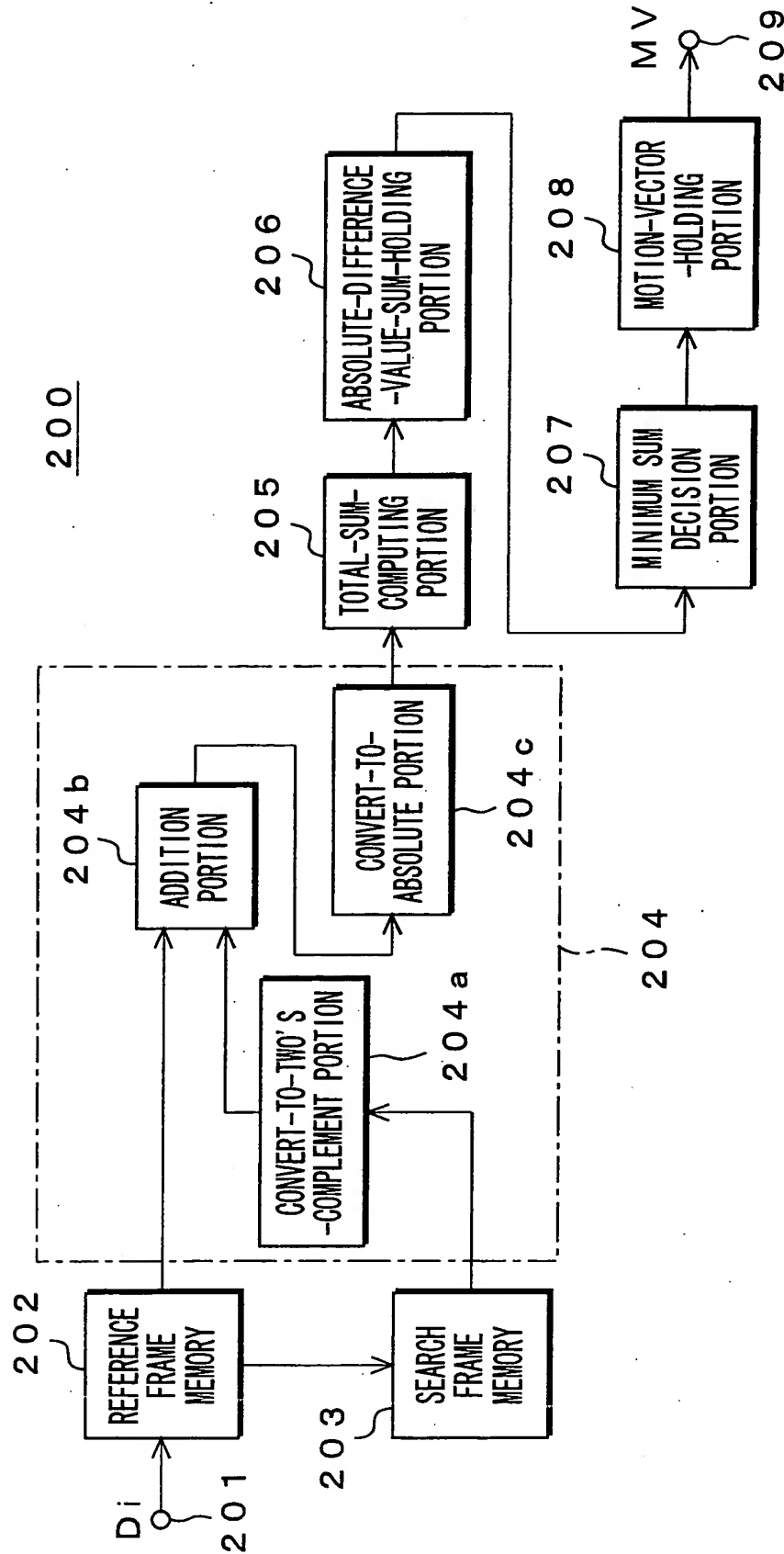
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F I G . 2



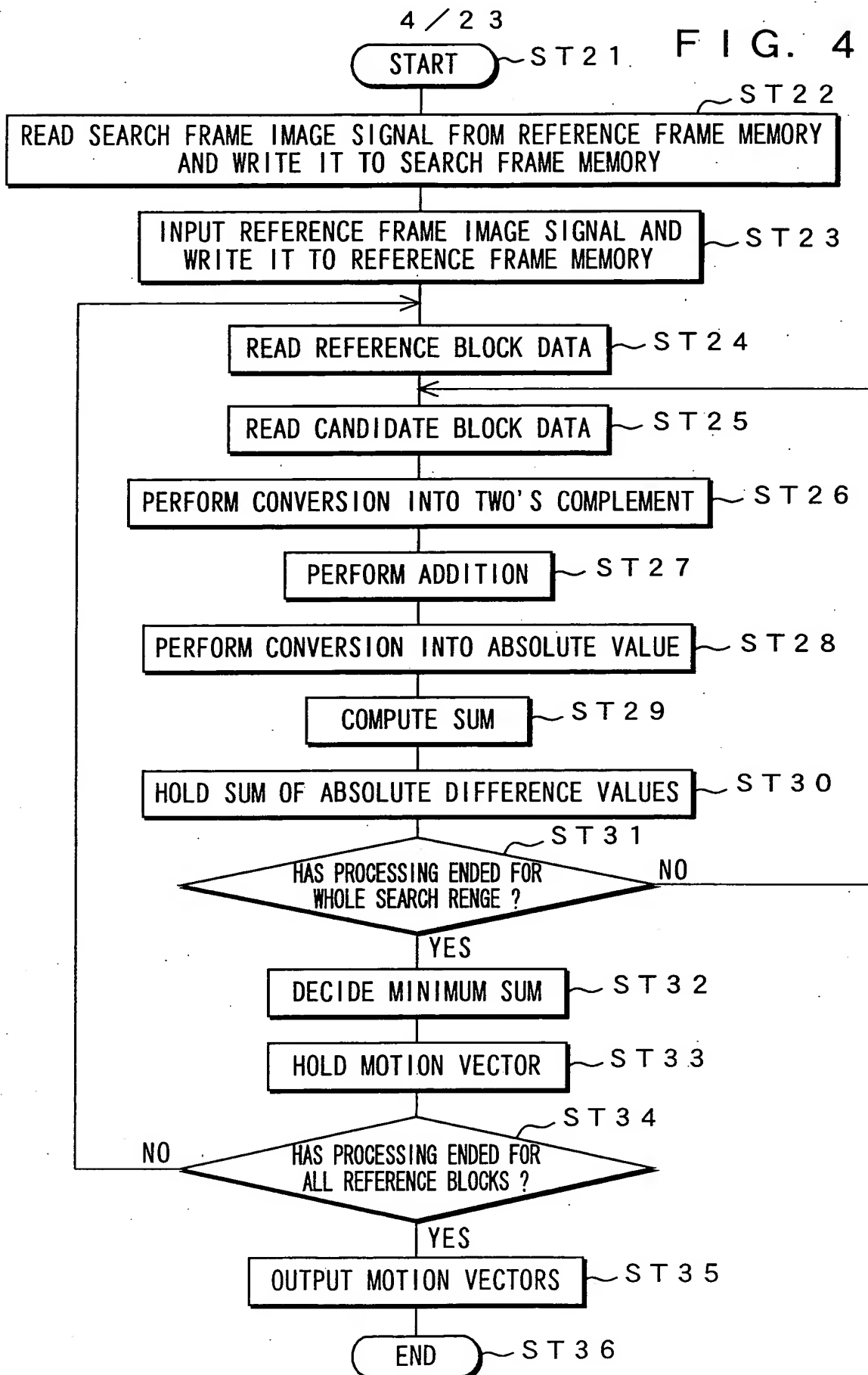
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FIG. 3



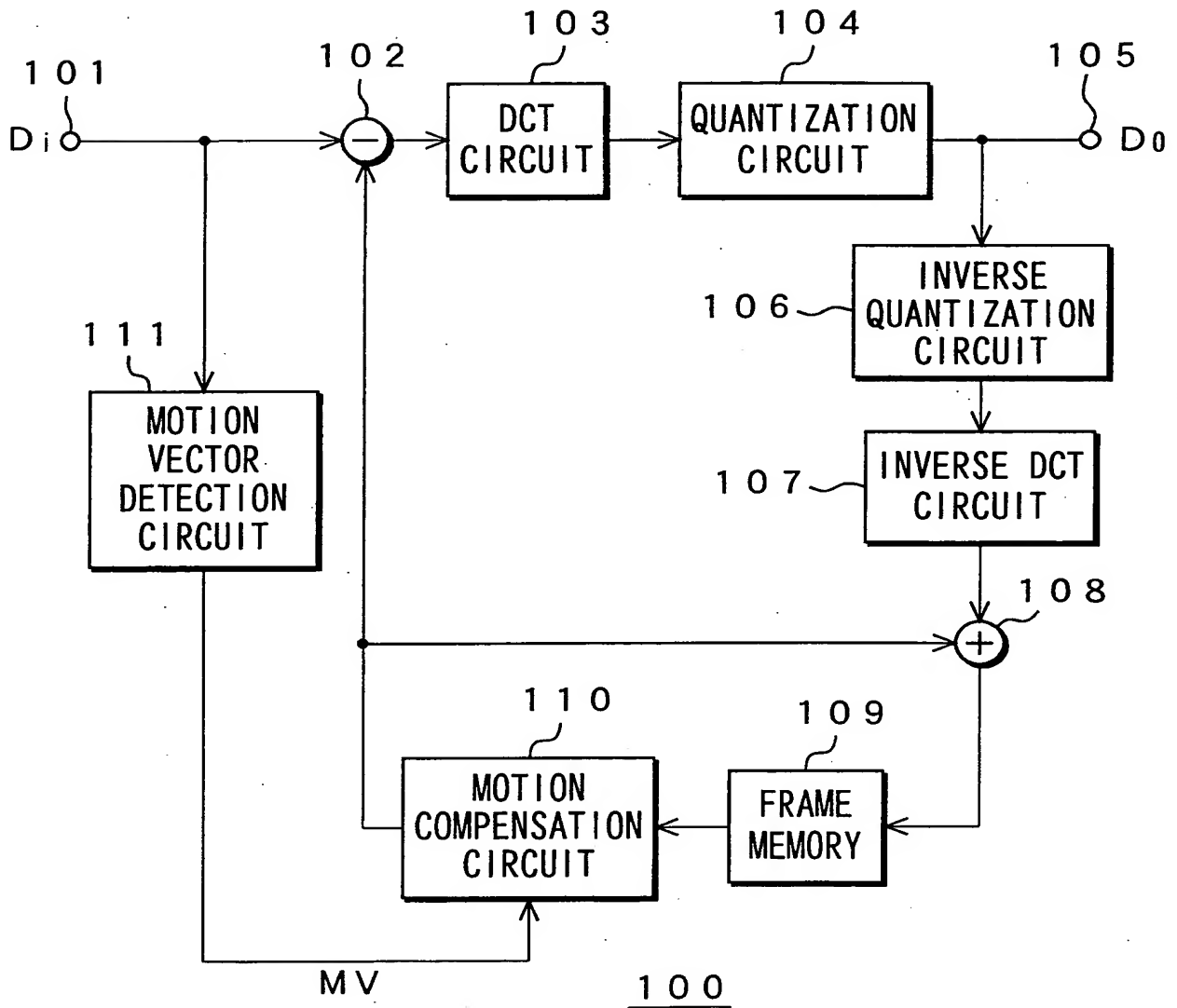
4 / 2 3

FIG. 4



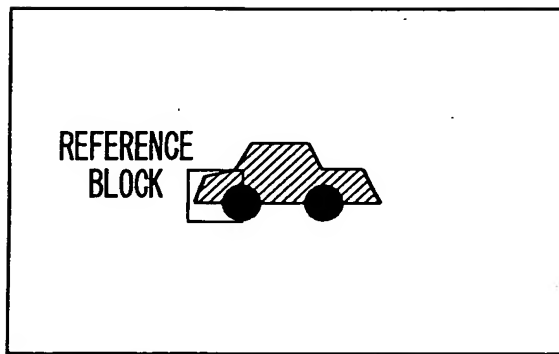
5 / 2 3

FIG. 5

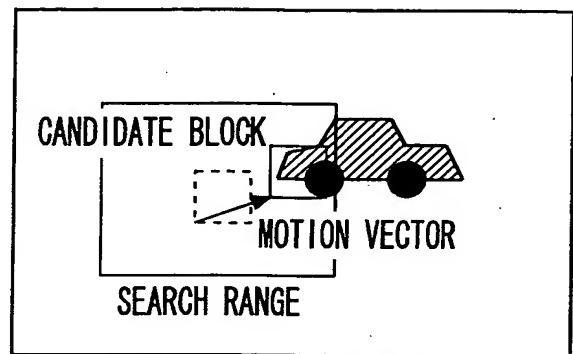


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FIG. 6



REFERENCE FRAME



SEARCH FRAME

FIG. 7 A

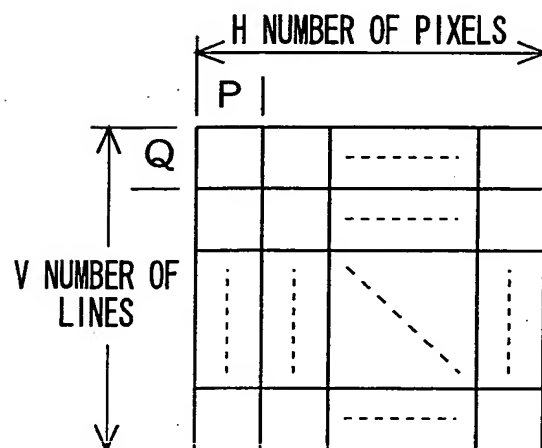
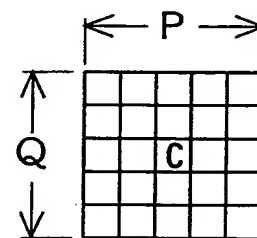


FIG. 7 B



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FIG. 8A

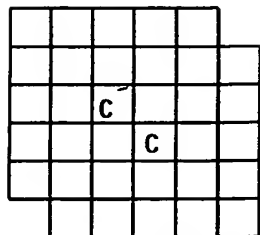


FIG. 8B

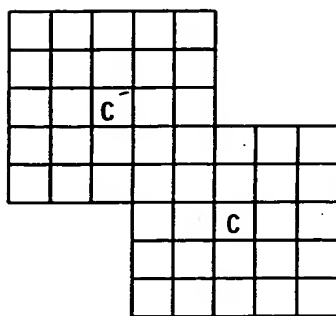


FIG. 8C

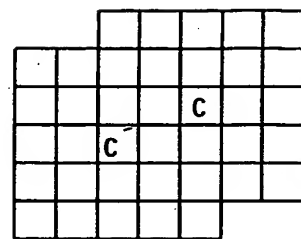
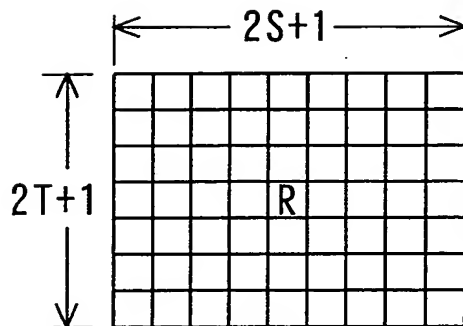
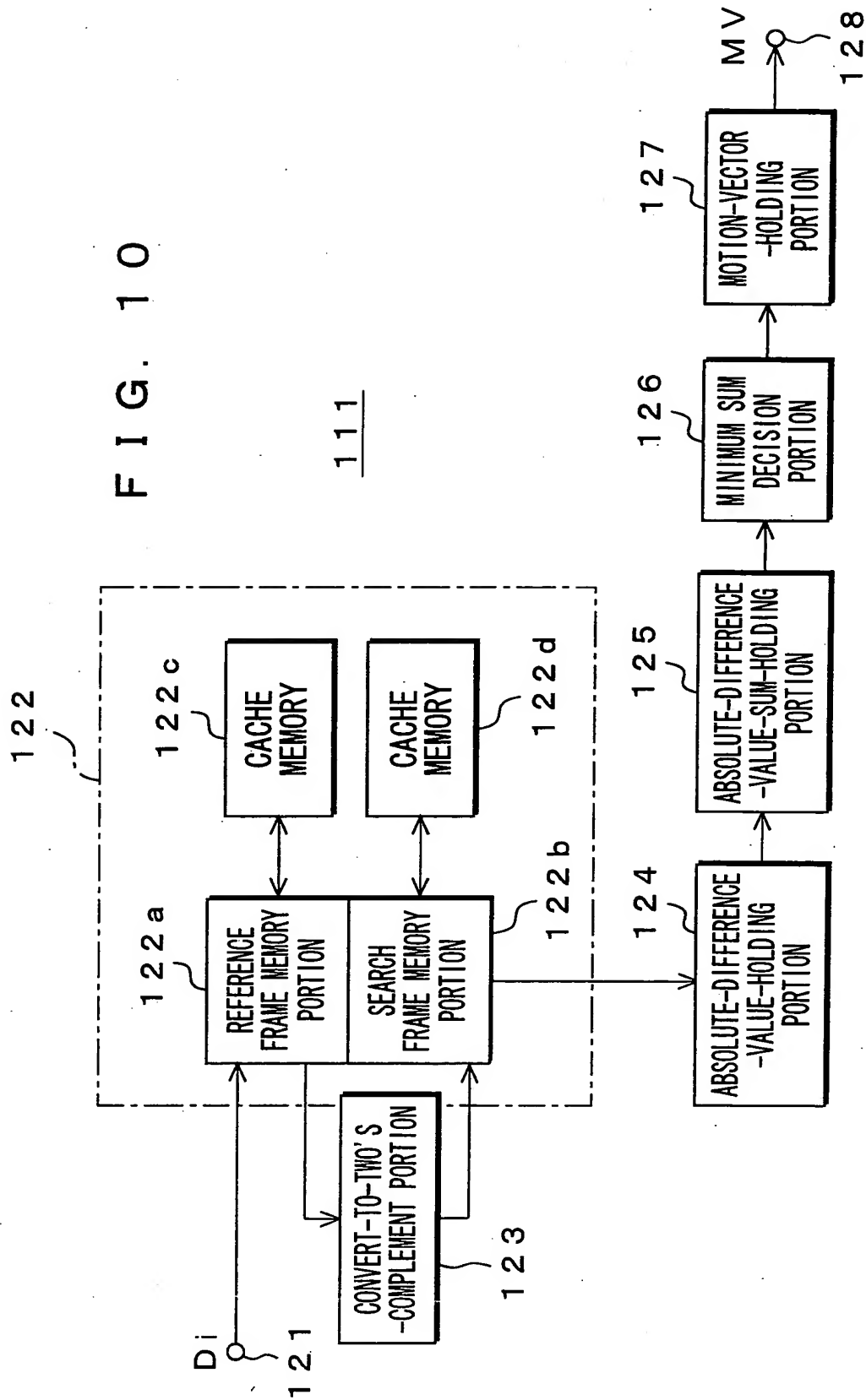


FIG. 9



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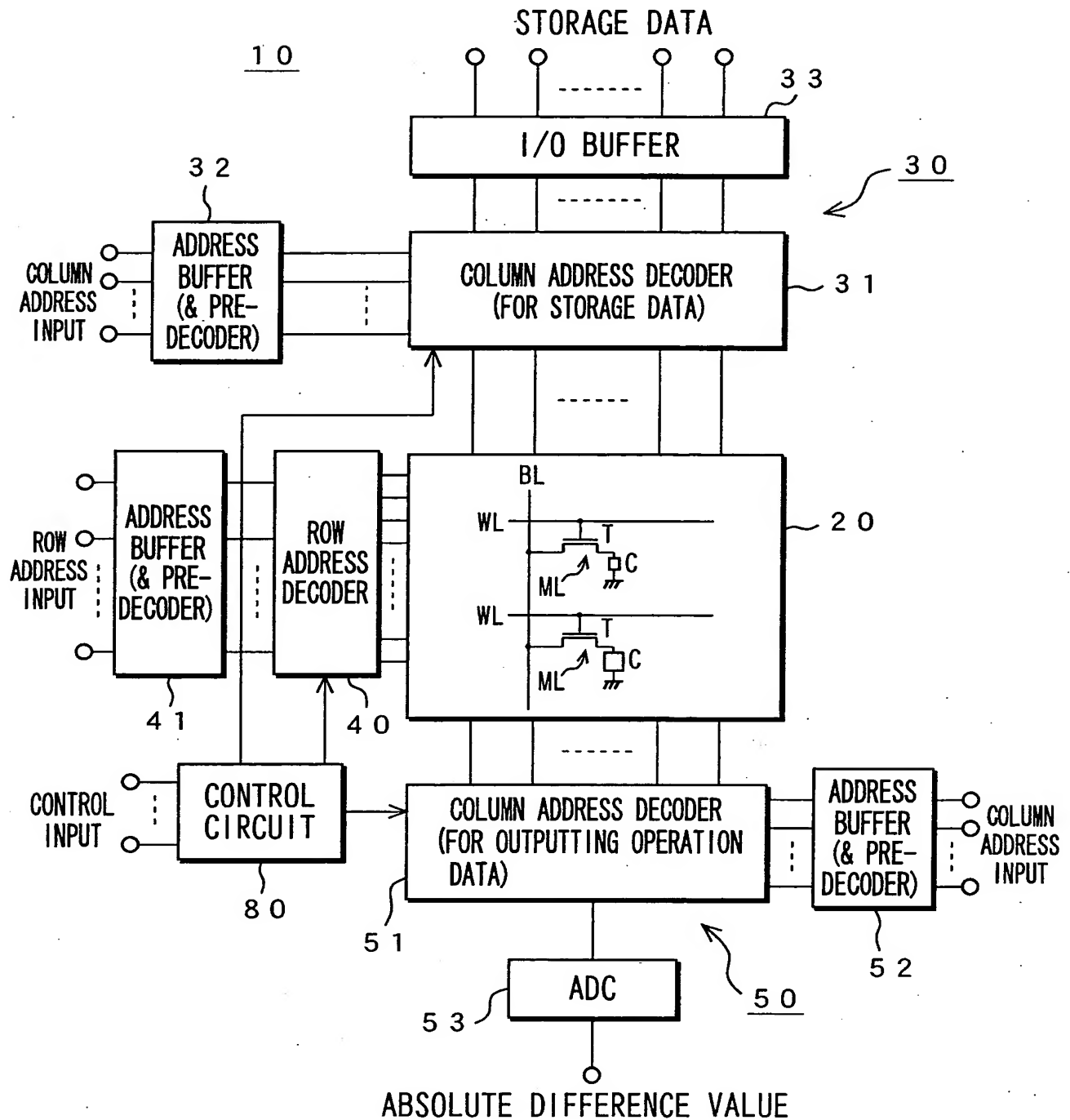
FIG. 10





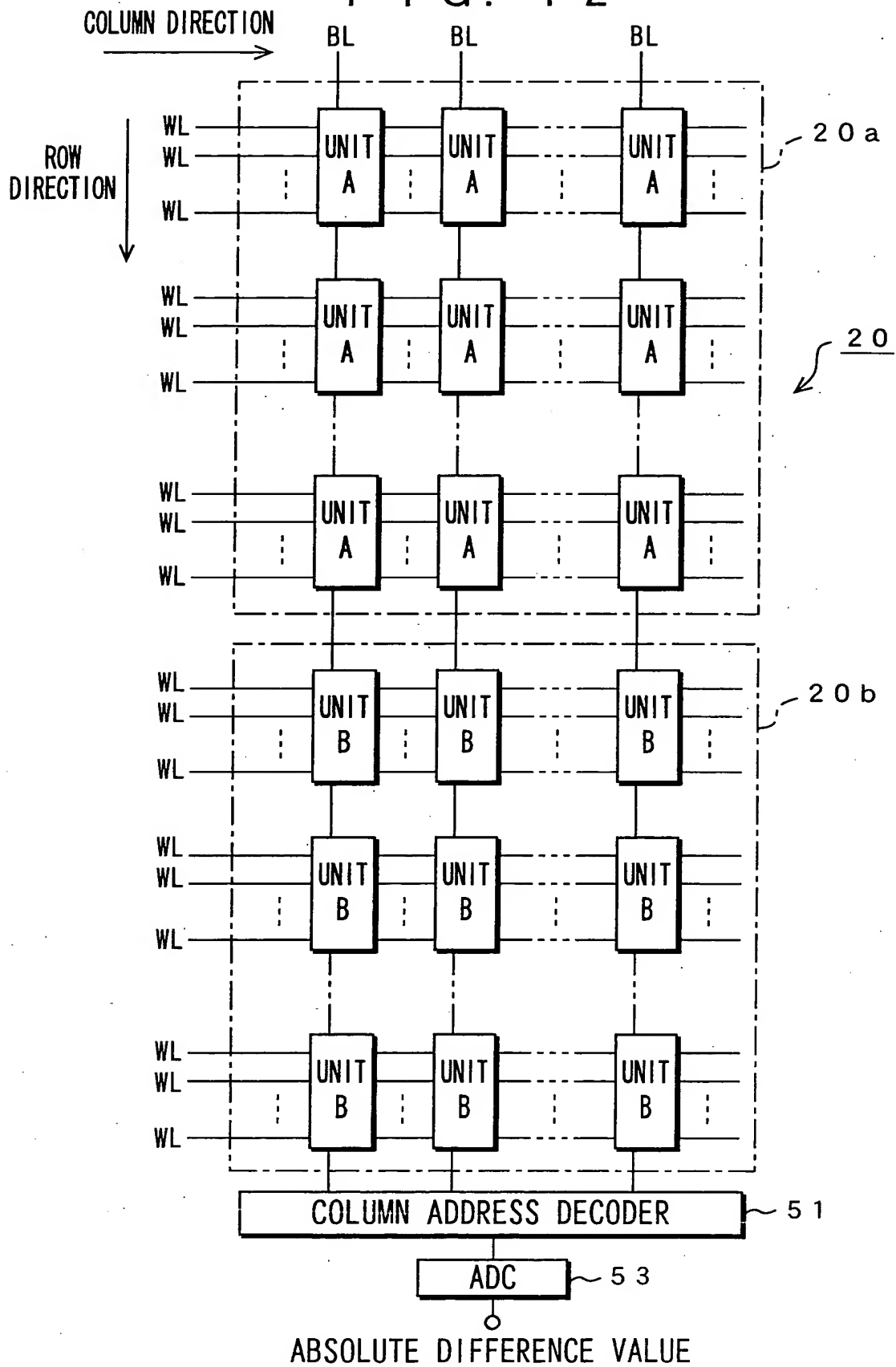
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F I G . 1 1



1 0 / 2 3

FIG. 12



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FIG. 13A

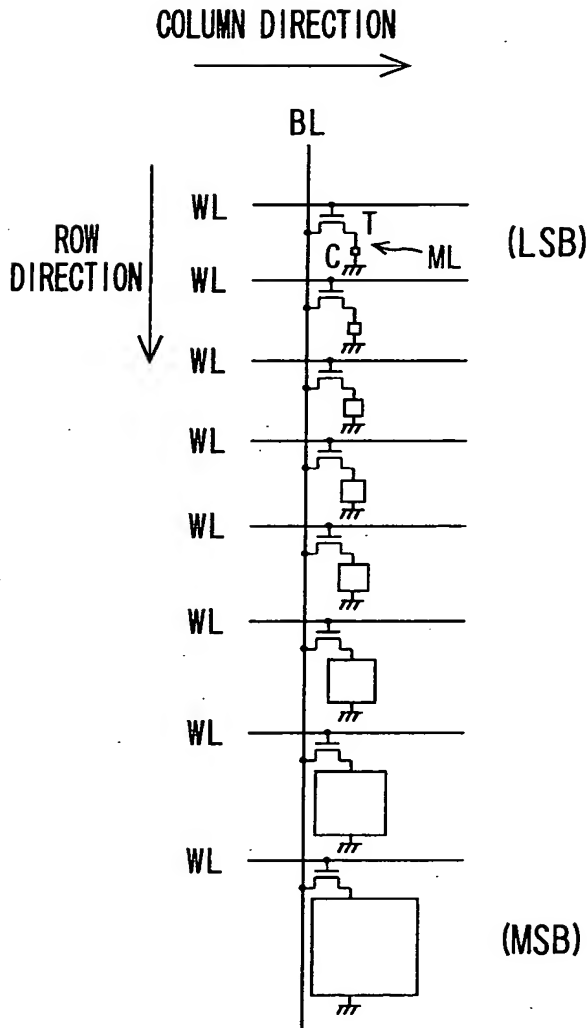
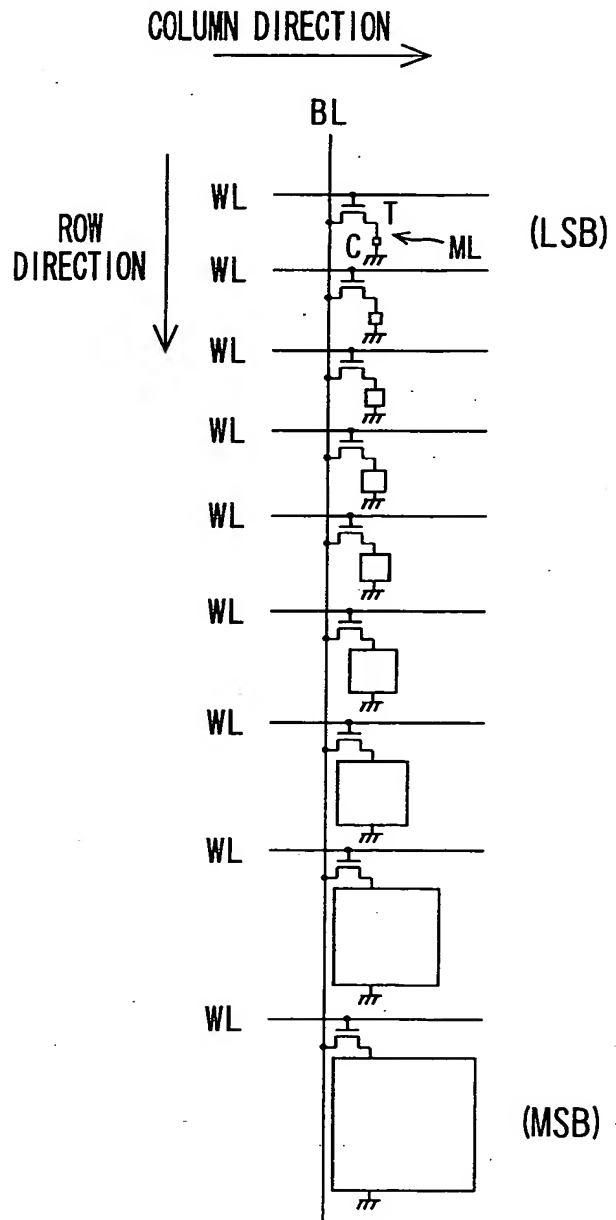
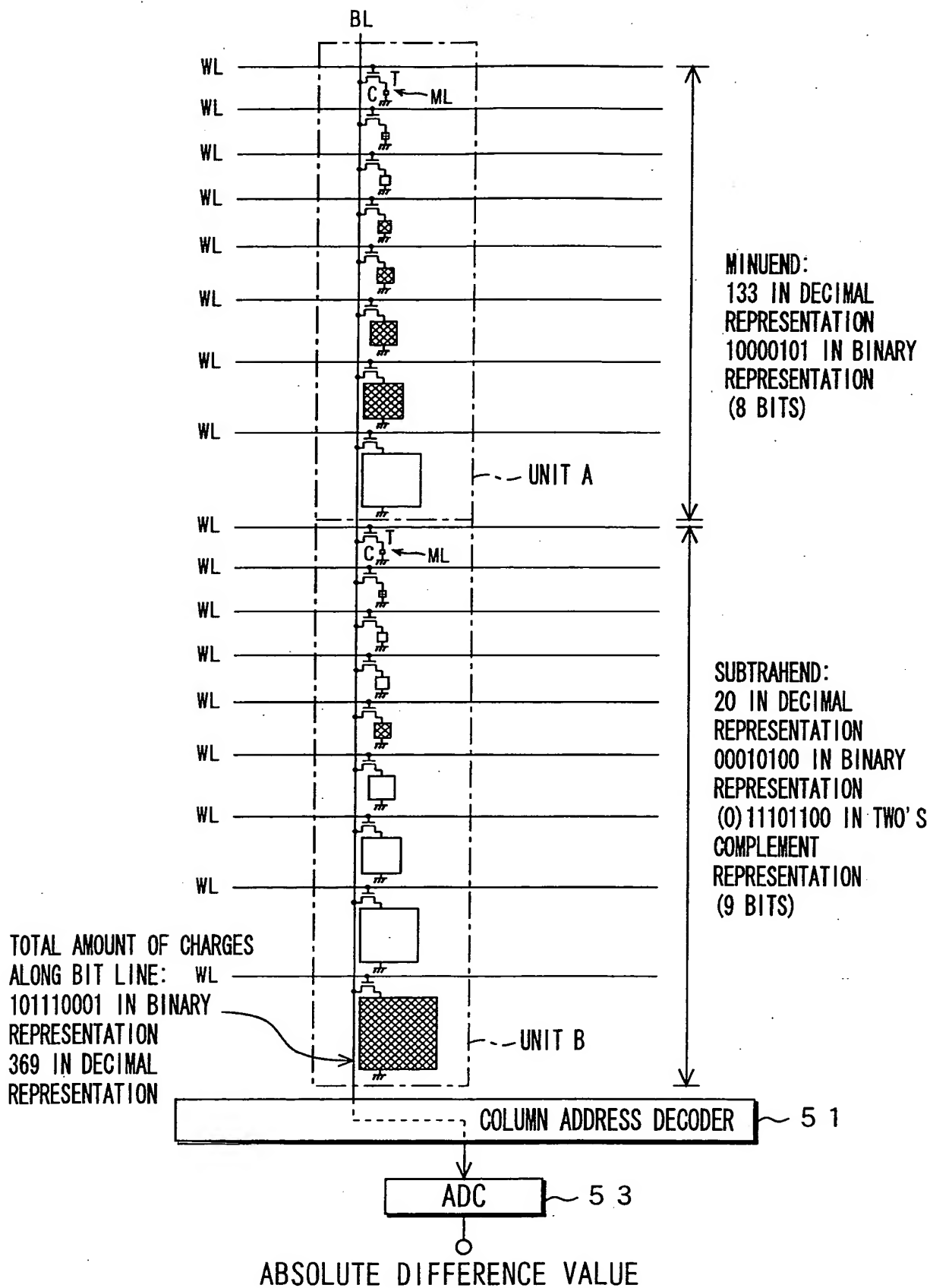


FIG. 13B

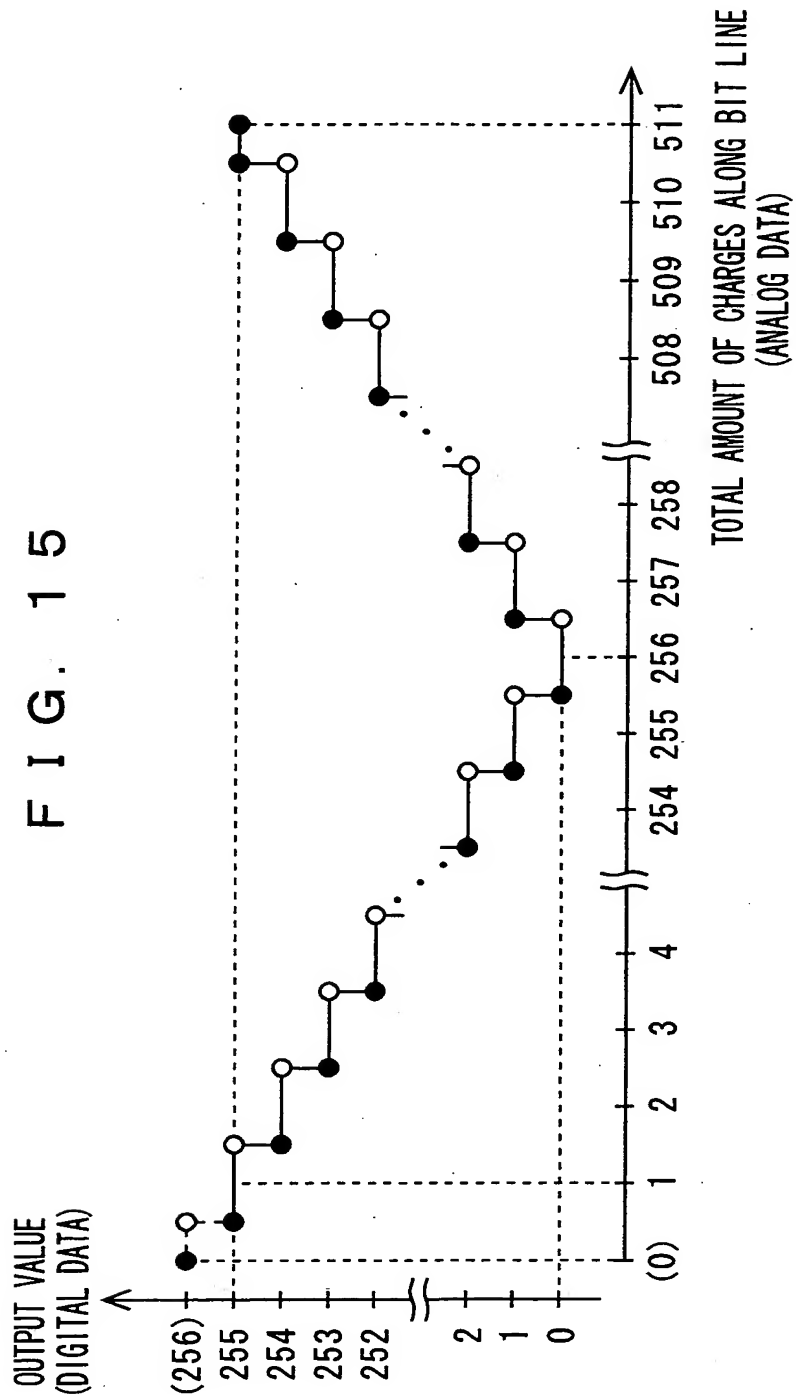


1 2 / 2 3

FIG. 14

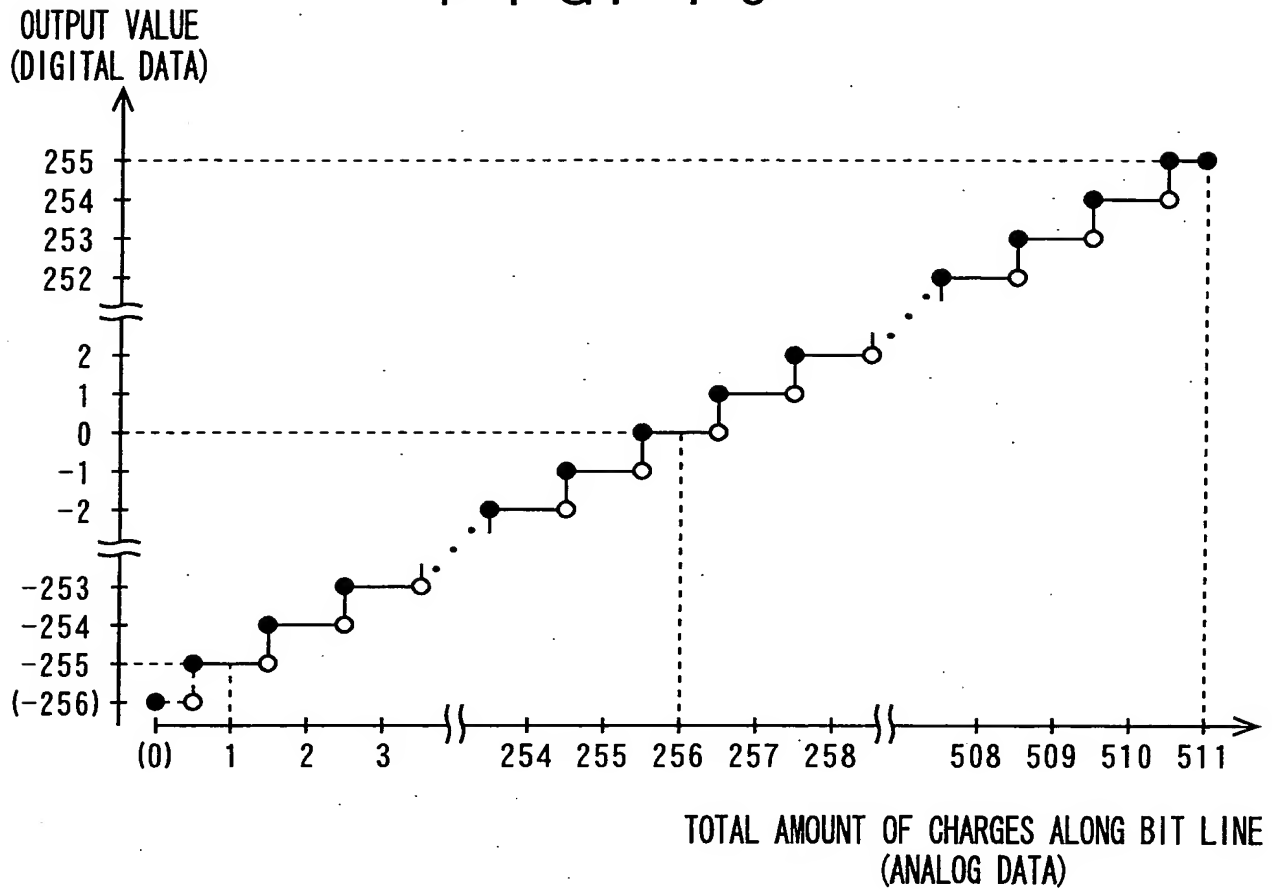


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1 4 / 2 3

F I G. 1 6



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FIG. 17

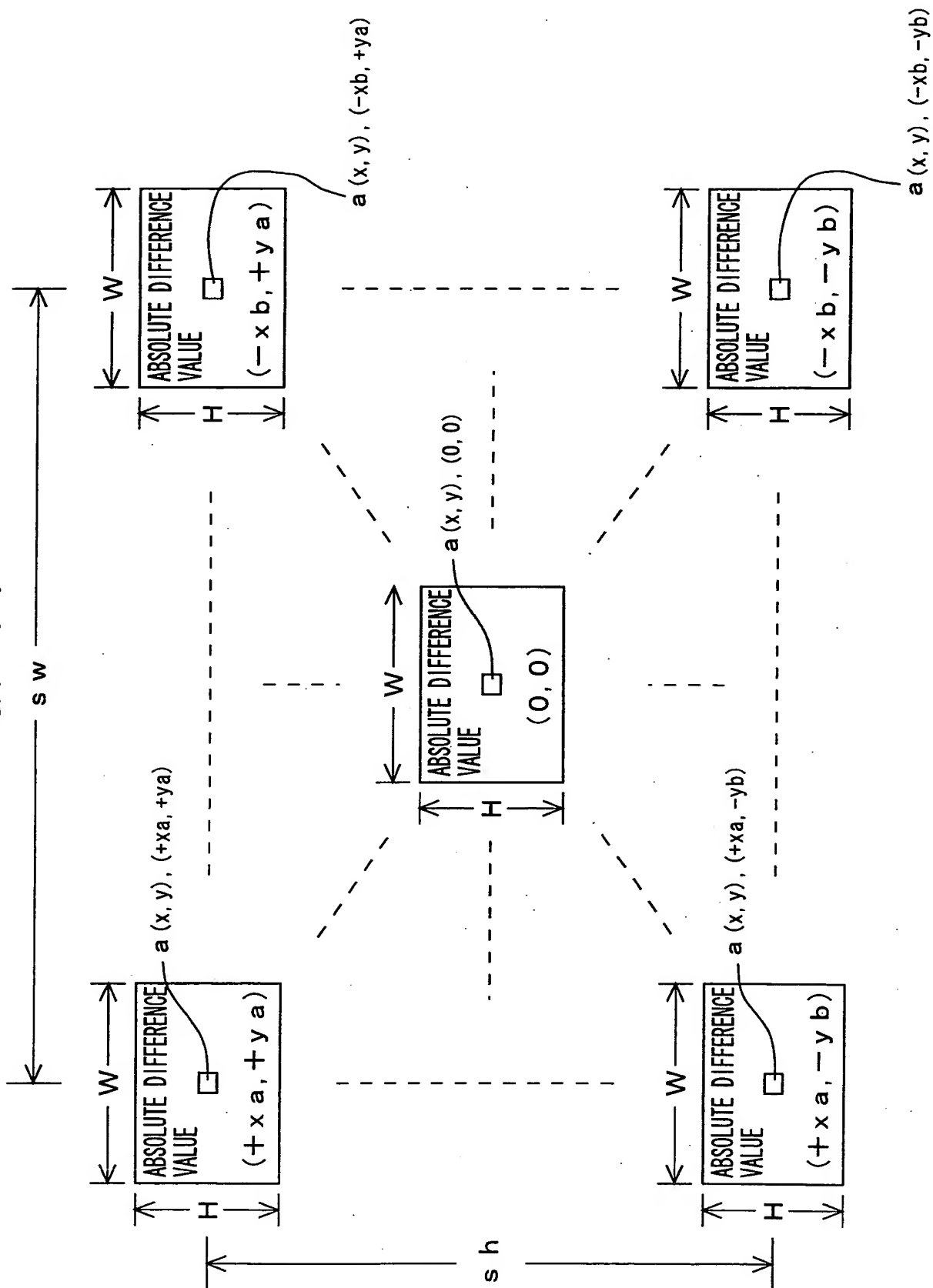
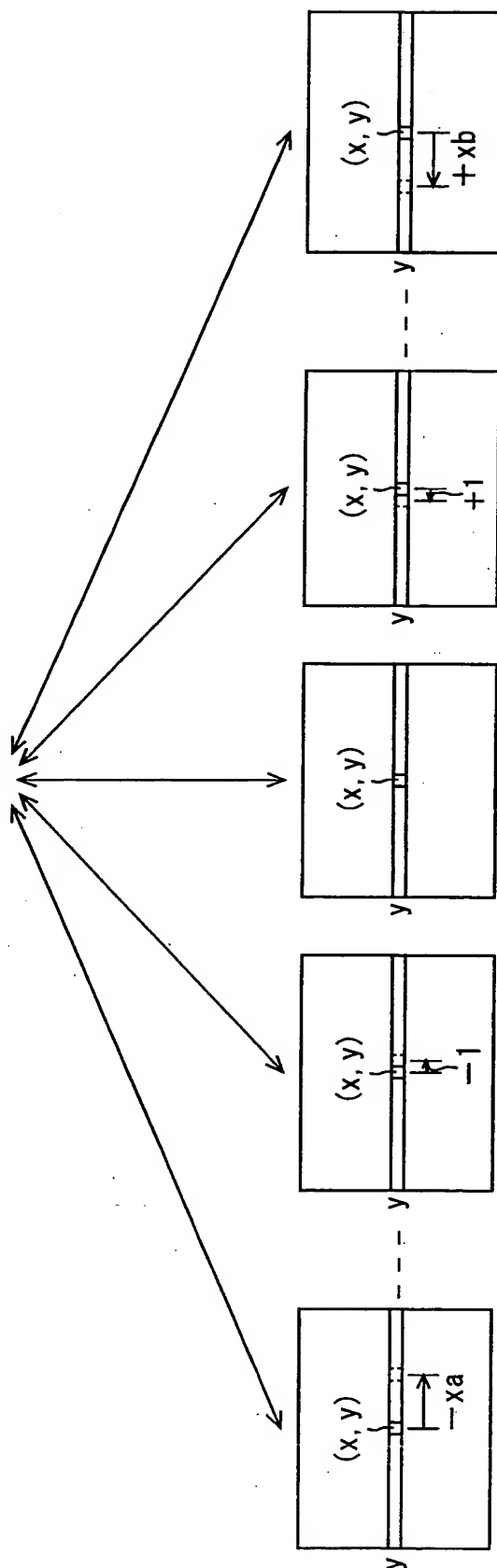
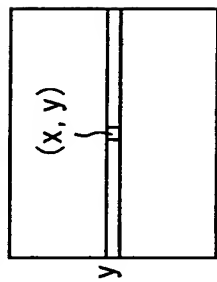


FIG. 18

REFERENCE FRAME

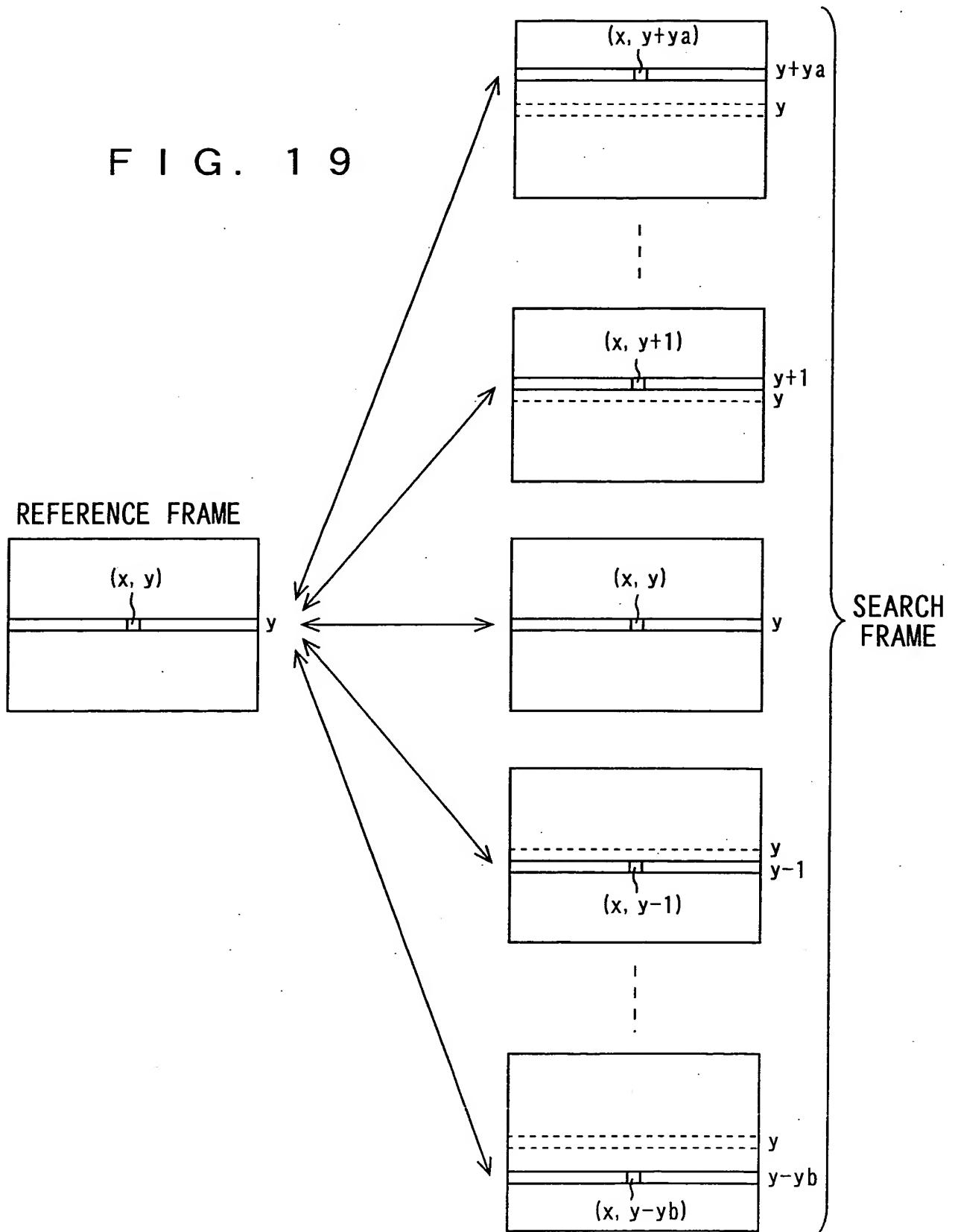


SEARCH FRAME



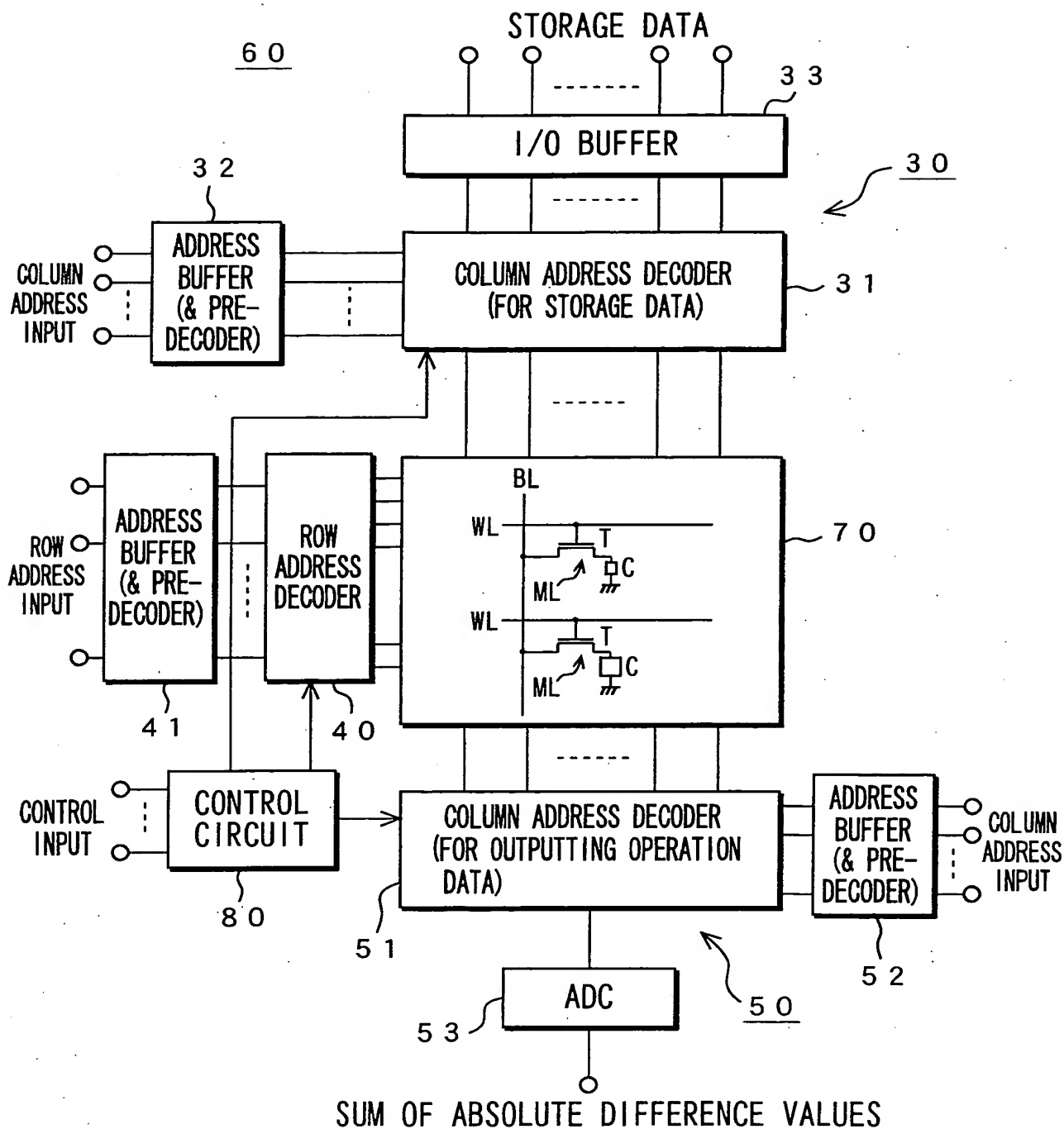
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FIG. 19



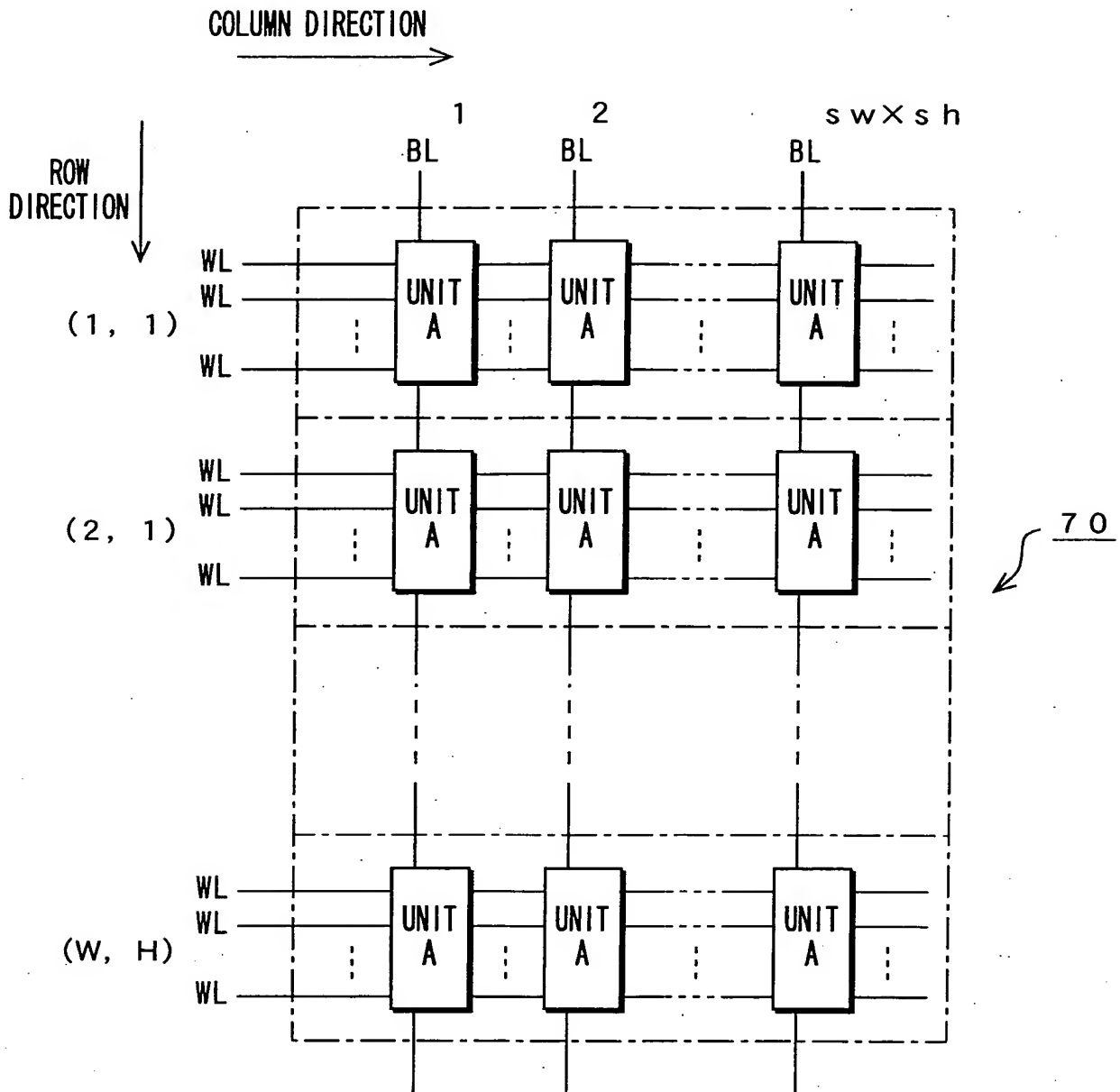
1 8 / 2 3

F I G . 2 0



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FIG. 21



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## FIG. 22

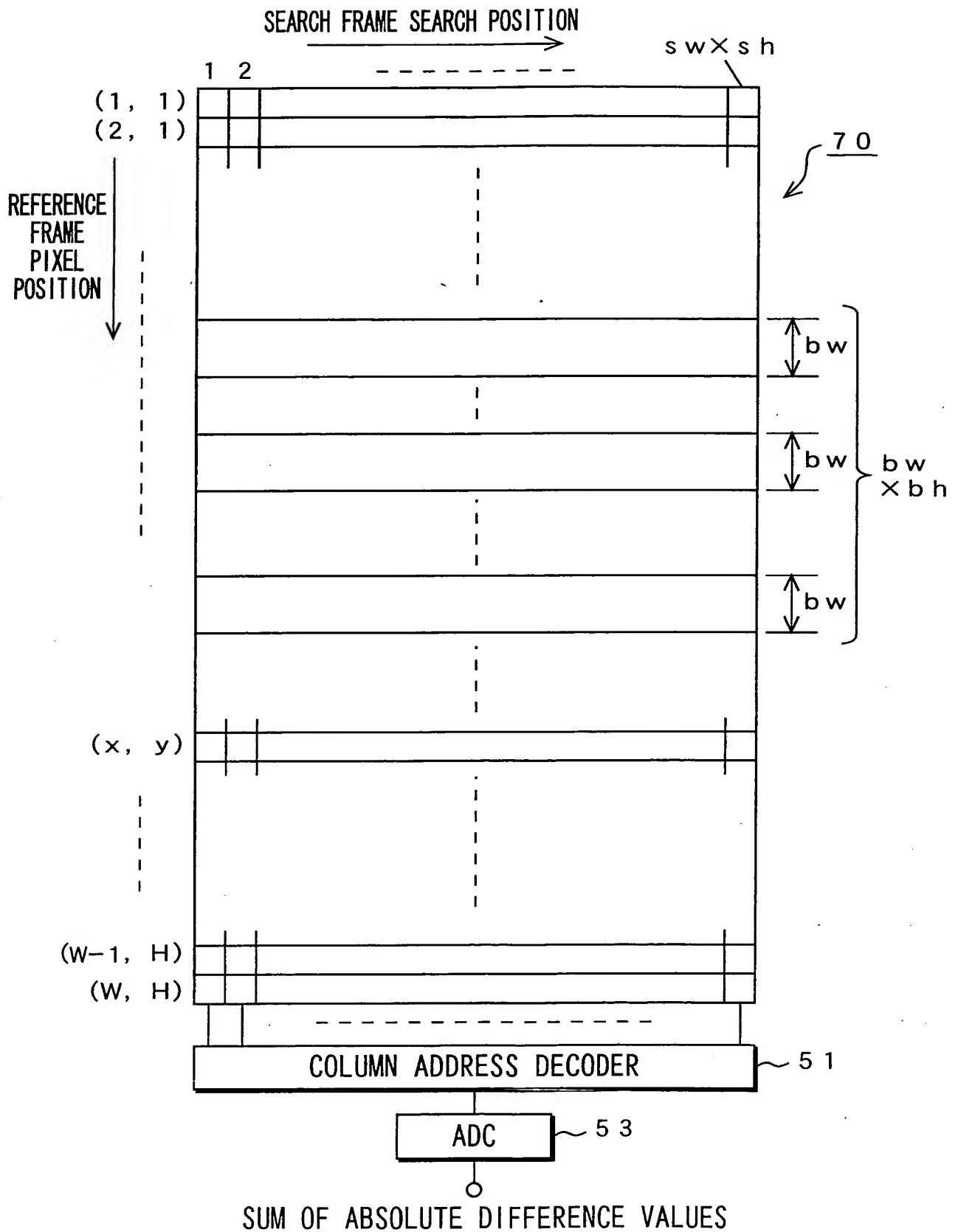


Diagram illustrating a 16-bit digital-to-analog converter (DAC) using a bit line architecture.

The diagram shows 16 word lines (WL) and a central bit line (BL). The bit line is divided into two sections by a break symbol. The top section contains 8 units (A1) and the bottom section contains 8 units (A2). Each unit is a 1-bit DAC.

**UNIT A1 (Top 8 units):**

- WL 1: 0 (no charge)
- WL 2: 0 (no charge)
- WL 3: 0 (no charge)
- WL 4: 0 (no charge)
- WL 5: 0 (no charge)
- WL 6: 0 (no charge)
- WL 7: 1 (charge)
- WL 8: 1 (charge)

**UNIT A2 (Bottom 8 units):**

- WL 9: 0 (no charge)
- WL 10: 0 (no charge)
- WL 11: 0 (no charge)
- WL 12: 0 (no charge)
- WL 13: 1 (charge)
- WL 14: 1 (charge)
- WL 15: 1 (charge)
- WL 16: 0 (no charge)

**TOTAL AMOUNT OF CHARGES ALONG BIT LINE:**

10011001 IN BINARY REPRESENTATION  
153 IN DECIMAL REPRESENTATION

**RIGHT SIDE ADDENDS:**

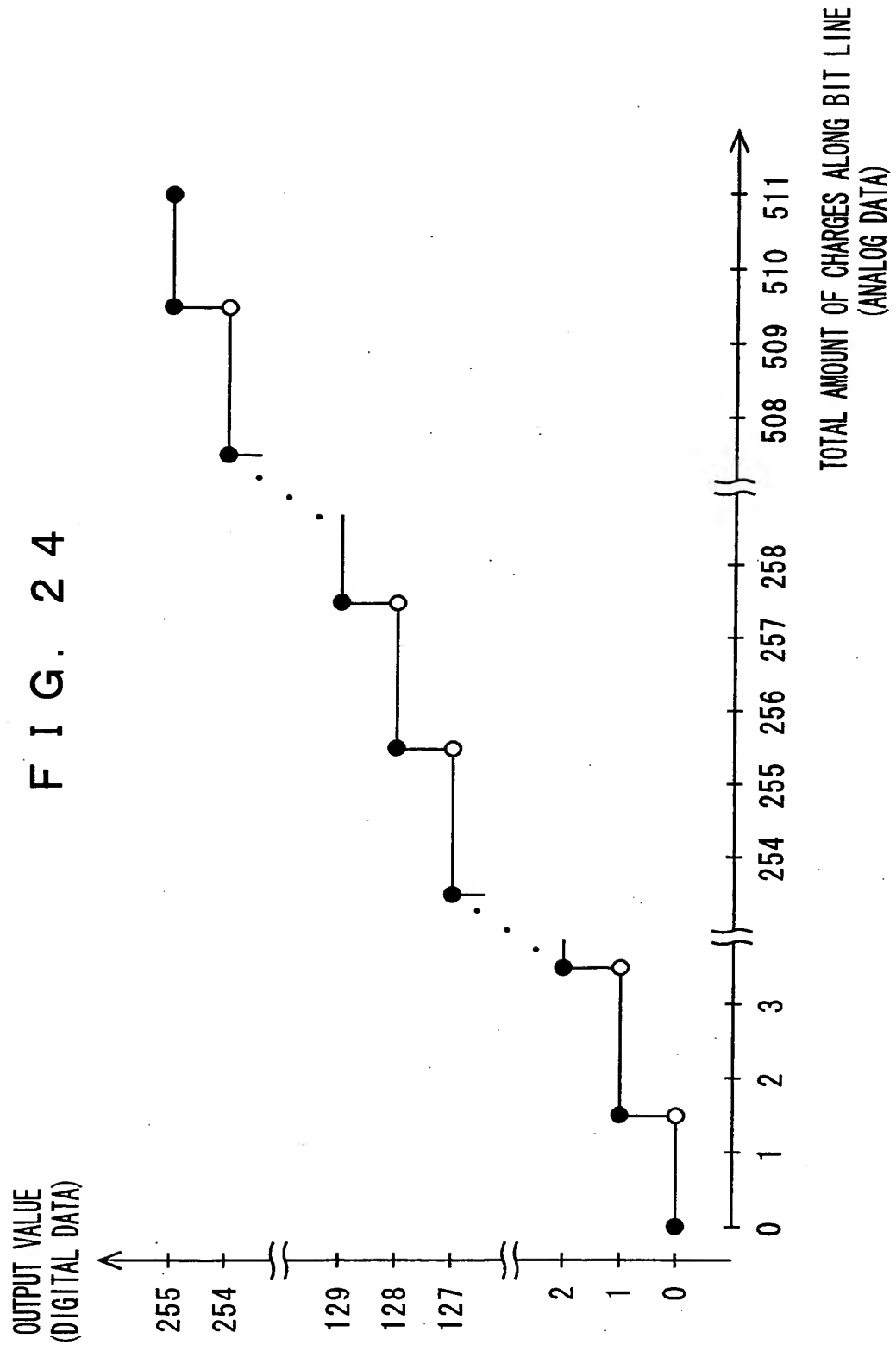
AUGEND:  
20 IN DECIMAL REPRESENTATION  
00010100 IN BINARY REPRESENTATION (8 BITS)

ADDEND:  
10000101  
133 IN DECIMAL REPRESENTATION  
10000101 IN BINARY REPRESENTATION (8 BITS)

The diagram also shows a COLUMN ADDRESS DECODER (5 1) and an ADC (5 3) block, which outputs the ADDED-UP DATA.

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FIG. 24



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FIG. 25

